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RESEARCH ARTICLE

# MODIFIED PRE-ENCODER FOR ETI CODING SCHEME

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**ABSTRACT**

Serial communications are more efficient to parallel communications as we humans are advancing to an age where every electronic devices are to be as portable as possible, the use of parallel buses needs to be avoided since these increases the requirement of space on a die. ETI schemes are now a days used for serial communications, the merit of which is to reduce the switching activity. This coding scheme is better that that of TIC scheme, which consumes more power. In this paper we are modifying the ETI-Pre encoder in encoding part to that of its predecessor, which resulted in power reduction. The simulations are done in Xilinx.



## INTRODUCTION

**A**s technological advancement takes place The system on chip design has gained mass acceptance in the field of large scale design. The system on chip design deals with the integration of millions of transistors into a single chip. The two main constraints for the system on chip design process are, the limited area of the chip in which the system have to be implemented and the power dissipation parameter. To tackle the issue of space and power consumption various schemes where proposed and one among them was to multiplex parallel busses into serial link The process of multiplexing parallel busses into serial links deals with the replacement of parallel busses ,which occupy larger area ,by serial links. The serialization process reduces inter connect area, coupling capacitance and crosstalk which was a cause of concern in parallel buses but resulted in larger switching activity hence larger power. The activity switching factor tends to increase with the increase in bit transitions.

This paper introduces a modified design of the Pre-Encoder section of Embedded transition inversion coding which reduces the area and power consumption than previous ones. The Second Section gives a brief idea about works in the field of reduction of activity switching factor and power dissipation when the multiplexing of parallel buses into a serial link is done. The Third Section presents the Pre-Encoder of ETI coding scheme. The process of ETI encoding is also explained in this chapter. Pre-encoder architecture is explained in Fourth in which architecture is divided into the proposed ETI encoder and Existing Pre-encoder decoder. Fifth section gives a brief conclusion.

### Previous Works

There are many techniques which are used to reduce serial links. This chapter gives an overview of the bus invert coding, the weight based bus invert coding, the partial bus invert coding, the serialized low energy transmission coding ,the transition inversion coding. The main advantage of the techniques about which we will be discussing in this chapter is that they were able to reduce the activity switching factor and also the power dissipation to an extent The main drawback of the techniques discussed below is the use of an extra bus. The required number of buses increases which increases the area overhead. The use of an extra bus to transmit the inversion information will again increase the energy requirement. The above bottlenecks of the previous techniques demanded a new method that solves the issues associated with them, the activity switching factor and the power dissipation.

#### *A. Bus Invert Coding (M. R. Stan and W. P. Burleson, Mar. 1995.)*

The bus invert coding technique reduces the activity switching factor by reducing the activity through the bus. That is the number of bit transitions is reduced. In the bus invert coding the term data value corresponds to the information bit or the

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data bit to be transmitted, and the term bus value corresponds to the information or the data through the bus. In the bus invert coding technique we use an extra bus which is called the invert bus. The invert bus either have a value ”0” which means the bus value will be equal to the data bit or a value “1” which means that the bus value will have a compliment value of the data bit. The value of the invert line is transmitted to the receiver side at all instances. The bus invert coding technique uses the hamming distance for deciding the value through the invert bus.

### *B. Weight Based Bus Invert Coding (R. B. Lin and C. M. Tsai, Jan. 2002,)*

The weight based bus invert coding technique is an advanced bus invert coding technique. The weight based bus invert coding technique aims to reduce the number of ones being transmitted through a bus. The weight based bus invert coding technique reduces the number of bit transitions. The weight based bus invert coding is similar to the bus invert coding method. The term data value corresponds to the information bit or the data bit to be transmitted, the term bus value corresponds to the information or the data through the bus and the term weight of data (**w**) which corresponds to the number of ones in a data value sequence. As in the bus invert coding technique here in the weight based bus invert coding technique we use an extra bus which is called the invert bus. The invert bus either have a value ”0” which means the bus value will be equal to the data bit or a value “1” which means that the bus value will have a compliment value of the data bit. The value of the invert line is transmitted to the receiver side at all instances .The main difference between the bus invert coding technique and the weight based bus invert coding technique is that the uses the weight of the data sequence instead of the hamming distance to compute the value through the through the invert bus.

### *C. PartialBus Invert Coding (Y. Shin, S. I. Chae, and K. Choi, Apr. 2001.)*

The partial bus invert coding technique is also an advanced bus invert coding technique. The partial bus invert coding technique aims to minimize the number of buses involved in bus coding. The partial bus invert coding technique enhances the reduction of overhead and also reduces the number of bit transitions. The term data value corresponds to the information bit or the data bit to be transmitted, the term bus value corresponds to the information or the data through the bus. As in the bus invert coding technique here in the partial bus invert coding technique we use an extra bus which is called the invert bus The invert bus either have a value ”0” which means the bus value will be equal to the data bit or a value “1” which means that the bus value will have a compliment value of the data bit. The value of the invert line is transmitted to the receiver side at all instances.

### *D. Serialized Low Energy Transmission Coding (K. Lee, S. J. Lee, and H. J. Yoo Nov. 2004)*

Serialized low energy transmission coding is commonly denoted as SILENT coding. The SILENT coding aims to minimize the transmission energy on the serial buses. The minimization of the transmission energy is achieved by minimizing the number of bit transitions through a bus and by minimizing the number of ones being transmitted through a bus. In SILENT coding scheme the parallel data bits on different buses are encoded and then serialized before transmission. The XOR operation is employed to encode and decode the data in the SILENT coding scheme. During the encoding process the present data bit and previous data bit is give as the inputs to a XOR gate. The output from the XOR gate is the encoded data bit. This process is done on all bit sequence to be transmitted. Once encoding is done the bit sequence is serialized and transmitted.

Once the data bits are received at the receiver, deserialization process is done. Now in order to retrieve the original data bits from the sender an XOR operation is employed. The presently received bit which is the encoded bit along with the previously decoded bit is given as the inputs to an XOR gate. The output of the gate gives the original data from the sender.

### E. *Transition Inversion Coding (R. Abinesh, R. Bharghava, and M. B. Srinivas, May 2009,* )

The transition inversion coding aims to reduce the number of transitions in a bit stream to be transmitted through a bus The transition inversion coding scheme reduces the energy consumption by reducing the total number of bit transitions and also reduces the activity switching factor. The total number of bits in a bit stream is referred to as the word length of a bit stream and is denoted as **W**. The term threshold value denoted as **N** corresponds to a value equal to the word length by two **(N**=**W**/2). The transition inversion coding scheme uses an extra indication signal called as transition inversion information indication bit. The transition inversion information indication bit denoted as **Bex.** The transition inversion information indication bit is transmitted through a bus called the transition inversion indication bus. The transition inversion indication bit will either be a “0” or a “1”. When the data bits in the bit stream are inverted so as to reduce the number of bit transitions the value of the transition inversion indication bit is set as “1” and when data bits in the bit stream are not inverted the value of the transition inversion indication bit is set as “0”. The transition inversion indication bit value is transmitted at all instances

## ETI Architecture

*Design Consideration*

There are four types of bus schemes, including parallel (P), serial (S), encoding followed by serial (ES), and serial followed by encoding (SE) as shown in Fig. 1.

The ES scheme is a good choice for applications, such as microprocessors or video processing based on the comparison of the four schemes shown in Fig. 1. The ES and SE coding schemes in Fig. 1 are both based on XOR operation that is suitable for bit streams with distinct values in adjacent bits. By replacing the XOR operation with our proposed ETI coding in the SE scheme, the switching activity of our proposed ETI

scheme is lower than the ES scheme for microprocessors or video processing..

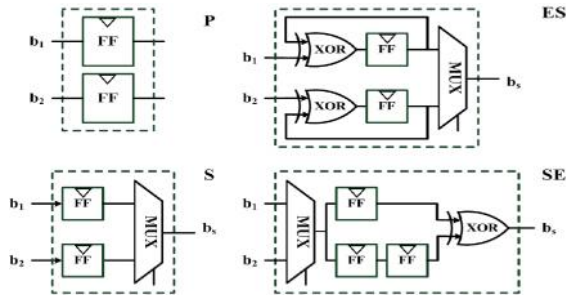


**Fig.1** Four types of bus schemes: P, S, ES, and SE

Although many coding algorithms can reduce the switching AF, most of them are designed for specific applications, such as video streaming or strongly correlated data. The TIC is one of the methods developed for random data . This method adds a transition indication bit to every data word to indicate if there is an inversion or not. This inversion coding is performed on every bit of two consecutive bits in the serial stream. The extra indication bit increases the switching activity. This paper proposes the ETI encoding scheme that operates on a two-bit basis and removes all the transition indication bits.

An n/m ETI serial links with n input bit streams under degree of multiplexing m is shown in Fig. 2. Each serial link has m input bitstreams that are multiplexed by a serializer, followed by the ETI encoding. The encoded stream is transmitted through the serial link and followed by the ETI decoding and a deserializer. The ETI coding scheme includes the inversion coding and phase coding as shown in Fig. 3.

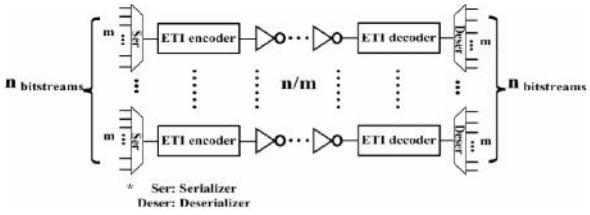


**Fig. 2** n/m ETI serial links with n input bitstreams under degree of multiplexing m.

1) Inversion Coding: Define the word length (WL) as the number of bits in a data word and a threshold Nth as half of WL. A transition is defined as a bit changing from zero to one or from one to zero. For example, the bitstream "0100" has two transitions while "0101" has three transitions. When the number of transitions Nt in a data word exceeds the threshold Nth, the bits in the data word should be encoded. Otherwise, the data word remains the same. When an encoding is needed in a data word, this method checks every two-bit in the data word, as Fig. 3 shows.

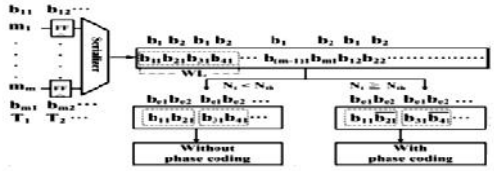


**Fig. 3** ETI coding scheme for one serial link, word length = WL, Nth = WL/2, and number of transition = Nt .

Every two bit in the serial stream is combined as a base to be encoded. In this case, the b11b21 is a base and the b31b41 is another base. The 2-bit in a base is denoted as b1b2 and the encoded output is denoted as be1be2. When the Nt in a data word is less than Nth, b1b2 remains unchanged. Otherwise, we perform the inversion coding and the phase coding. For the inversion coding, the bitstreams "01" and "10" are mapped to "00" and "11," respectively. The bitstreams "00" and "11" are mapped to "01" and "10," respectively. For the phase coding, we embed the inversion information in the phase difference between the clock and the encoded data.

The inversion encoding operation can be expressed as

$$be1 = b1$$
$$be2 = \begin{cases} \overline{b2}, & \text{with } Nt \geq Nth \\ b2, & \text{with } Nt < Nth \end{cases} \quad (1)$$

**Table1** All Combinations Of Two Bit streams For The TIC, ETIpre Schemes and ETI

| Parallel streams | | | | Serial Stream TIC | Serial stream $ETI_{pre}$ | Serial stream ETI |
|---|---|---|---|---|---|---|
| Stream1 | | Stream 2 | | | | |
| $b_{11}$ | $b_{12}$ | $b_{21}$ | $b_{22}$ | | | |
| 0 | 0 | 0 | 0 | 0000**0** | 0000 | 0000 |
| 0 | 0 | 0 | 1 | 0001**0** | 0001 | 0001 |
| 0 | 0 | 1 | 0 | 0100**1** | 0100 | 0100 |
| 0 | 0 | 1 | 1 | 0011**0** | 0011 | 0011 |
| 0 | 1 | 0 | 0 | 0001**1** | 0001 | 0001 |
| 0 | 1 | 0 | 1 | 0000**1** | 0000 | **1**000 |
| 0 | 1 | 1 | 0 | 0011**1** | 0011 | 0011 |
| 0 | 1 | 1 | 1 | 0111**0** | 0111 | 0111 |
| 1 | 0 | 0 | 0 | 1000**0** | 1000 | 1000 |
| 1 | 0 | 0 | 1 | 1100**1** | 1100 | 1100 |
| 1 | 0 | 1 | 0 | 1111**1** | 1111 | **0**111 |
| 1 | 0 | 1 | 1 | 1110**1** | 1110 | 1110 |
| 1 | 1 | 0 | 0 | 1100**0** | 1100 | 1100 |
| 1 | 1 | 0 | 1 | 1000**1** | 1000 | 1000 |
| 1 | 1 | 1 | 0 | 1110**0** | 1110 | 1110 |
| 1 | 1 | 1 | 1 | 1111**0** | 1111 | 1111 |

***PRE-ENCODER***

***Existing Encoder***

The overall architecture of the ETI scheme is shown in Fig. 4 ETI are divided mainly into two, ETI encoder and ETI decoder. The ETI does not provide the decision bit information so it cannot be decoded in the receiver. The ETI pre encoder is shown by the dashed box in the ETI encoder in Fig. 4. The TIC counts the transitions in the data word then uses this information to perform encoding. The transition indication bit is added to every data word to indicate whether there is an inversion or not.

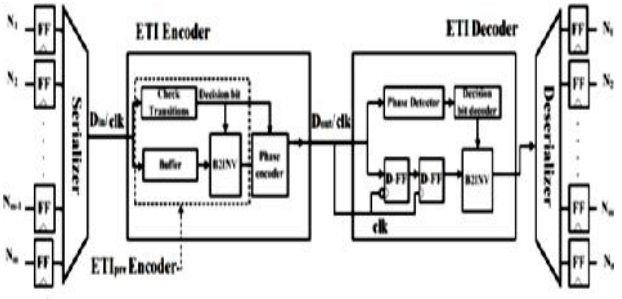


**Fig. 4** ETI Block.

In the ETI encoder part, the input data Din are stored in the buffer to wait until the check transition operation is completed.

The transition and threshold in a data word are used to set the decision bit. The decision bit is used to control the encoding process in the B2INV and the phase encoder block. When the decision bit is set to zero, the B2INV passes the noninverted bitstream. Otherwise, the bitstream is encoded. The ETI encoder includes the check transitions block, buffer,B2INV and Phase Encoder.

**Check Transitions Block**

The check transition block is shown in Fig. 5. The WL indicator block counts the length of the data word and generates a high signal at the first bit of the data word. This signal is used to reset the adder and the D-flip-flop (D-FF). The D-FF stores the previous bit that is used to XOR with the current bit for transition checking. The adder block calculates the number of transition in a data word and sets the decision bit to high when the Nt ≥ Nth . The check transition block in Fig. 5, which is used to detect the number of the transitions, is part of the ETI encoder.

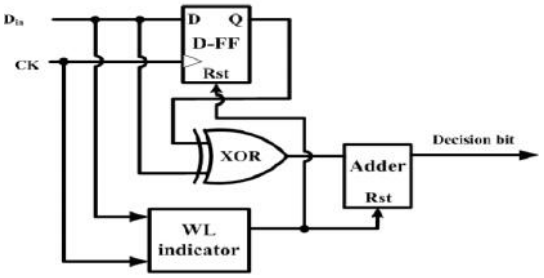


**Fig. 5** Check transition block

**B2inv Block**

The architecture of the B2INV is shown in Fig. 5. The divider, which divides the clock by two, provides an indication signal for the first or second bit in a pair of bitstream b1b2. If it is the first bit, then the bit passes through. Otherwise, the bit is inverted when the decision bit is high.

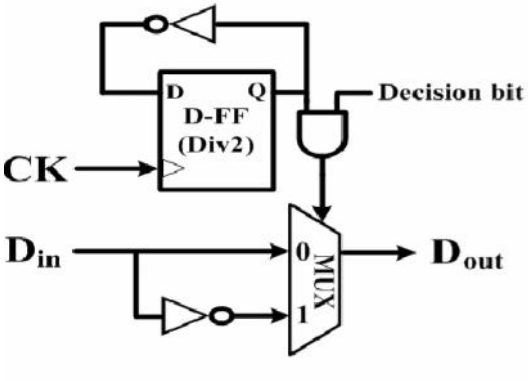


**Fig. 6** B2INV block.[9]

***Buffer Block***

This block generates delay in the process so that the decision bit can coagulate the input data to create a perfect timing for the decision bit to map an input to the B2INVERSION block. It consist of the Memory which helps to provide the necessary delay for the decision bit to reach the B2INV block at the same time the input is included.

***Proposed Pre-Encoder***

The Word Length Indicator used in proposed method is removed. Since, the Word Length Indicator and the Dflip Flop in the Check Transition Block uses the same inputs and WLI is only used to indicate the initial bit the WLI block is removed and in place we use the Control Block. Which creates a Control signal used to communicate with the Adder block in the Check Transition Block hence reducing the size and power dissipation. Latter a simpler buffer is created using D Flip-Flops which further reduces the power consumption which is analyzed using the XPower Analyzer. The modified Check Transition Block is shown below.

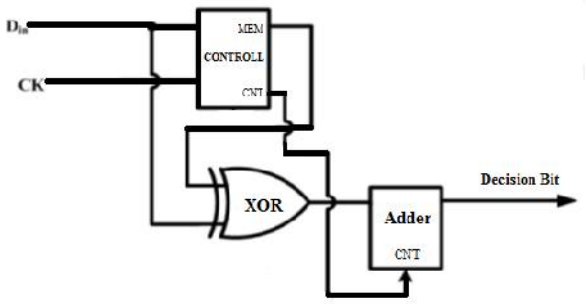


**Fig. 7** Check transition block

**Table 2** Comparison of Existing and Proposed Pre-Encoder

| | **Existing Pre-Encoder** | **Proposed Pre-Encoder** |
|---|---|---|
| Number of Slice Flip Flops | **47** | **35** |
| Number of 4input LUTs | **52** | **40** |
| Number of IOs | **3** | **3** |
| Maximum Frequency | **172.087MHz** | **196.928MHz** |
| Power Delay product | **581.1 µWnS** | **406.4µWnS** |

## CONCLUSION

The proposed method will help to reduce the delay and power to an considerable extent. Thus the main problem in serialization that is the power consumption can be tackled.

## References

K. Lee, S. J. Lee, and H. J. Yoo, "SILENT: Serialized low energy transmission coding for on-chip interconnection networks," in Proc. *IEEE Int. Conf. Comput.-Aided Design Conf.*, Nov. 2004, pp. 448–451.

M. R. Stan and W. P. Burleson, "Bus-invert coding for low-power I/O," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 3, no. 1, pp. 49–58, Mar. 1995.

Y. Shin, S. I. Chae, and K. Choi, "Partial bus-invert coding for power optimization of application-specific systems," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 9, no. 2, pp. 377–383, Apr. 2001.

R. B. Lin and C. M. Tsai, "Weight-based bus-invert coding for low power applications," in Proc. *Int. Conf. VLSI Design*, Jan. 2002, pp. 121–125

S. R. Sridhara and N. R. Shanbhag, "Coding for reliable on-chip buses: A class of fundamental bounds and practical codes," *IEEE Trans. Comput.- Aided Design Integr. Circuits Syst.*, vol. 26, no. 5, pp. 977–983, May 2007

K. Lee, S. J. Lee, and H. J. Yoo, "Low-power network-on-chip for high performance SoC design," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 2, pp. 148–160, Feb. 2006.

R. Narasimha and N. Shanbhag, "Design of energy-efficient high-speed links via forward error correction," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 5, pp. 359–364, May 2010.

P. Subrahmanya, R. Manimegalai, V. Kamakoti, and M. Mutyam, "A bus encoding technique for power and cross-talk minimization," in Proc. *IEEE Conf. VLSI Design*, Jun. 2004, pp. 443–448.

Ching-Te Chiu, Wen-Chih Huang, Chih-Hsing Lin, Wei-Chih Lai, and Ying-Fang Tsao "*Embedded Transition Inversion Coding With Low Switching Activity for Serial Links*" IEEE transactions on very Large Scale Integration (VLSI) systems, vol. 21, no. 10, october 2013

B. Razavi, "Challenges in the design of high-speed clock and data recovery circuits," IEEE Commun. Mag., vol. 40, no. 8, pp. 94–101, Aug. 2002.

R. Abinesh, R. Bharghava, and M. B. Srinivas, "Transition inversion based low power data coding scheme for synchronous serial communication," in Proc. IEEE Comput. Soc. Annu. Symp. VLSI Conf. May 2009, pp. 103–108.

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