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## RESEARCH ARTICLE

# DESIGN & OPTIMIZATION OF LOW POWER TURBO DECODER FOR WIRELESS SENSOR NETWORKS

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### ABSTRACT

In the Wireless Sensor Networks, turbo decoders have recently been considered for energy-constrain, since they facilitate low transmission energy consumption. However, in order to reduce the overall energy consumption, lookup table-log-BCJR (LUT-Log-BCJR) architectures having low processing energy consumption are required. In this proposed technique, the LUT-Log-BCJR architecture along with fundamental Add Compare Select (ACS) operations which performed by using a novel low-complexity ACS unit. The architecture employs an order of magnitude fewer gates than the most recent LUT-Log-BCJR architectures. The proposed technique will reduce nearly 10% of total power consumption.

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## INTRODUCTION

Wireless Sensor Networks (WSN) has gained growing research interest in the last years. It is shown that in WSNs the transmission energy can be lowered accepting to receive error-affected data. In this case the receiver should embed error correction strategies to recover the original data [1,2]. In particular, the amount of energy spent to perform error correction should be significantly lower than the energy saved at the transmitter side.

As an example, an energy efficient error correction scheme for WSNs is proposed. In particular, the physical layer of the IEEE 802.15.4 standard is augmented introducing interleaving and forward error correction. Several classes of codes are investigated, including Reed-Solomon codes, convolution codes, turbo codes and Low-Density-Parity-Check (LDPC) codes [6,7]. Experimental results show that LDPC codes are good candidates for WSN applications as they feature a significant coding gain as compared with other codes. This motivates the employment of the lookup-table-log BCJR (LUT-Log-BCJR) algorithm in energy-constrained scenarios,

since it approximates the optimal Log-BCJR more closely than the Max-Log-BCJR and therefore does not suffer from the associated coding gain degradation. However, to the best of our knowledge, no LUT-Log-BCJR ASICs have been specifically designed for energy-constrained scenarios. Previous LUT-Log-BCJR turbo decoder designs were developed as a part of the on-going drive for higher and higher processing throughputs, although their throughputs have since been eclipsed by the Max-Log-BCJR architectures. This opens the door for a new generation of LUT-Log-BCJR ASICs that exchange processing throughput for energy efficiency. In the paper decompose the LUT-Log-BCJR architecture into its most fundamental add compare select (ACS) operations and perform them using a novel low-complexity ACS unit. We demonstrate that our architecture employs an order of magnitude fewer gates than the most recent LUT-Log-BCJR architectures, facilitating a 71% energy consumption reduction [3,4,5].

### Existing System

The Wireless Sensor Networks (WSNs) can be considered to be energy constrained wireless scenarios since the sensors are operated for extended periods of time, while relying on

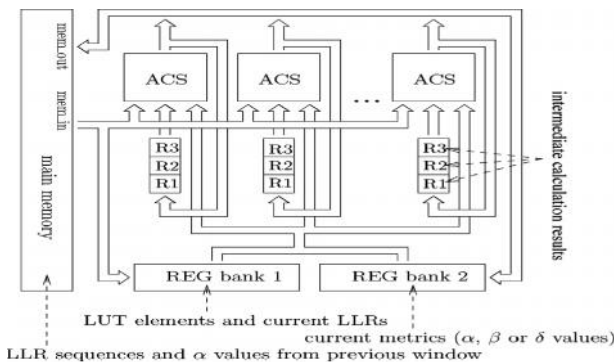
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batteries that are small, lightweight and inexpensive. The Max-Log-BCJR algorithm appears to lend itself to both high-throughput scenarios, as well as to the above-mentioned energy-constrained scenarios. This is because low turbo decoder energy consumption is implied by Max-Log-BCJR algorithm's low complexity. However, this is achieved at the cost of degrading the coding gain by 0.5 dB compared to the optimal Log-BCJR algorithm increasing the required transmission energy by 10%. As this disadvantage of the Max-Log-BCJR outweighs its attractively low complexity, when optimizing the overall energy consumption of sensor nodes that are separated by dozens of meters [8,9,10].

**Proposed System**

Propose a novel LUT-Log-BCJR architecture for energy-constrained scenarios, which avoids the wastage of energy that is inherent in the conventional architecture. Our philosophy is to redesign the timing of the conventional architecture in a manner that allows its components to be efficiently merged. This produces an architecture comprising only a low number of inherently low-complexity functional units, which are collectively capable of performing the entire LUT-Log-BCJR algorithm. Further wastage is avoided, since the critical paths of our functional units are naturally shortened equally-lengthened, eliminating the requirement for additional hardware to manage them. Furthermore, our approach naturally results in a low area and a high clock frequency, which implies low static energy consumption.



**Fig 1** LUT-Log-BCJR-ACS

The above which is the proposed ACS unit Shown in fig 1 it is used to function very efficiently and gives of parallel output. It consists of the registers in order to store the bits. A turbo encoder comprises a parallel concatenation of two convolutional encoders, each of which has a structure comprising m number of memory elements, where m=3 is used in the LTE encoders, for example.

Each encoder converts an uncoded bit sequence  $b_1 = \{b_{1,j}\}_{j=1}^{N_j} = 1$  into the corresponding encoded bit sequence  $b_2 = \{b_{2,j}\}_{j=1}^{N_j} = 1$  where is the length of the input bit sequences. Correspondingly, Fig depicts a turbo decoder which comprises a parallel concatenation of two decoders, that employ the LUT-Log-BCJR algorithm. Rather than operating on bits, each LUT-Log-BCJR decoder processes Logarithmic Likelihood Ratios (LLRs), where each LLR  $b = \ln(p(9b-0)) / (p(b-1))$  quantifies the decoder's confidence concerning its estimate of a bit from the bit sequences and Each LUT-Log-BCJR decoder processes

two a priori LLR sequences, namely  $b'_1 = \{b'_{1,j}\}_{j=1}^{N_j} = 1$  and  $b'_2 = \{b'_{2,j}\}_{j=1}^{N_j} = 1$  which are converted into the extrinsic LLR sequence  $b_{1e} = \{b_{1e,j}\}_{j=1}^{N_j} = 1$ . This extrinsic LLR sequence is iteratively exchanged with that generated by the other LUT-Log BCJR decoder, which is used as the a priori LLR sequence  $b'_{1e}$  in the next iteration.

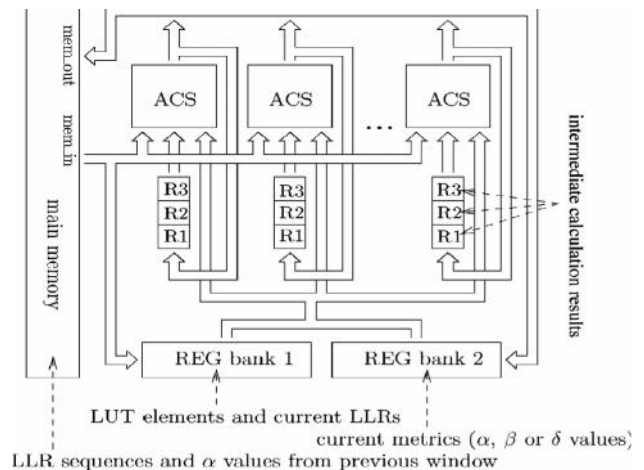
The conventional LUT-Log-BCJR architecture, which employs the sliding-window technique, to generate the LLR sequence as the concatenation of equal-length sub-sequences. Each of these windows is generated separately, using a forward, a pre-backward and a backward recursion.

**Energy-Efficient LUT-LOG-BCJR**

The proposed energy- efficient LUT-Log-BCJR architecture is unlike conventional architectures, it does not use separate dedicated hardware for the three recursions. Instead, our architecture implements the entire algorithm using ACS units in parallel, each of which performs one ACS operation per clock cycle. Furthermore, the proposed architecture employs a twin-level register structure to minimize the highly energy-consuming main-memory access operations. At the first register level, each ACS unit is paired with a set of general purpose registers R1, R2, and R3.

These are used to store intermediate results that are required by the same ACS unit in consecutive clock cycles. This motivates the employment of the lookup-table-log BCJR (LUT-Log-BCJR) algorithm in energy-constrained scenarios, since it approximates the optimal Log-BCJR more closely than the Max-Log-BCJR and therefore does not suffer from the associated coding gain degradation.

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**Fig 2** Energy Efficient LUT-Log-BCJR Architecture



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