International Journal Of

Recent Scientific Research

ISSN: 0976-3031

Volume: 7(2) February -2016

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THE OFFICIAL PUBLICATION OF
INTERNATIONAL JOURNAL OF RECENT SCIENTIFIC RESEARCH (IJRSR)
http://www.recentscientific.com/ recentscientific@gmail.com

ISSN: 0976-3031

Available Online at http://www.recentscientific.com

International Journal of Recent Scientific Research
Vol. 7, Issue, 2, pp. 9071-9074, February, 2016

International Journal of Recent Scientific Research

RESEARCH ARTICLE

DESIGN OF NOR CONTENT ADDRESSABLE MEMORY BIT CELL USING SHORTED GATE FINFETS

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ARTICLE INFO

Article History:

Received 15th November, 2015
Received in revised form 21st December, 2015
Accepted 06th January, 2016
Published online 28th February, 2016

Keywords:

Content addressable memories (CAMs), FinFET, Short channel Effects, Tanner EDA.

ABSTRACT

Content addressable memories (CAMs) are special type of computer memory that is used in search intensive applications. It involves content based searching. The conventional CAM is designed using MOSFET, due to which the power consumption is very high because of parallel architecture and short channel Effects such as leakage current. However, the current trend is to use new non planar device architecture, the so called FinFET to overcome the problems of planar MOSFET stated above. Among the alternatives to planar MOSFET, FinFET is proved to be more efficient in terms of power. This paper proposes a design of NOR content addressable memory bit cell using 22-nm shorted gate FinFETs. The design has been synthesized in 22nm technology using Tanner EDA tool.

INTRODUCTION

Content addressable memories (CAMs) are computer memories, also known as associative memory that search data based on content instead of explicit address. The data to be searched is given as input to the CAM, and then the CAM compares the input data with data previously stored in the lookup table. If the data is matched, it outputs the location of the matched data within a single clock cycle. Thus it is mainly used in applications that require high speed search operations such as in translation look-aside buffers (TLBs), network routers database accelerators, image processing, parametric curve extraction, Hough transformation, Lempel–Ziv compression, image coding, virus detection and Huffman coding/decoding[1],[2].

Because of this fast searching operation in CAMs, there will be high dynamic power consumption [3] [4].This was a major problem in the CAM designed in the past. But, due to advancements in CMOS technology, leakage in memories became a huge concern [5] [6]. As the transistors are scaled in nanoscale, transistors are kept very close to each other, which increases the parasitic effects between individual circuit node than the transient behavior of memory bit cells, such as SRAMs[7][8].

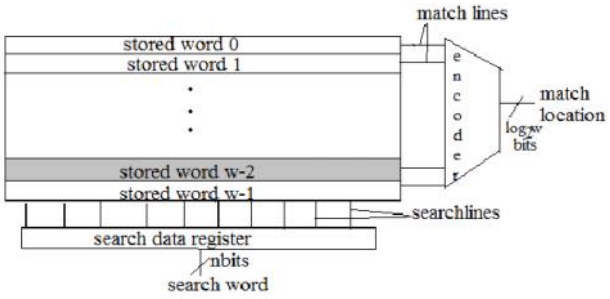

Fig 1 Block Diagram of Cam

When transistors are scaled to nanoscale, the conventional MOSFET started losing its property due to short channel effects. Multi-gate devices started replacing conventional MOSFETs. Double Gate FETs (DGFETs) are better substitute to planar MOSFETs as the two gates aid a better electrostatic control over the channel. FinFET is a type of DGFET that has better scalability and compatibility with the planar CMOS process [10], [11].

FinFETs are of three types, namely, Shorted Gate (SG),

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Asymmetric gate-work function Shorted –Gate (ASG), Independent Gate (IG). In the SG type FinFET, the two gates are shorted together and it yield largest ON current (I_{ON}).The ASG type FinFET is similar to shorted gate, but the two gates have different work functions. It has the same layout area as that of SG FinFET, and has lower leakage current achieved at the cost of 26% degradation in the drive current (I_{ON}). In IG FinFETs, the two gates are made independent by etching away the gate material above the vertical channel. Though the leakage current in IG FinFETs is one to two orders of magnitude lower than that of SG FinFETs (with appropriate back-gate bias), it is at the expense of a severe degradation in ION and increase in layout area due to the need to insert back-gate contacts[12]-[14].

Out of the three FinFETs, SG FinFET is fast but leaky and ASG FinFET is slower but less leaky. IG FinFETs are less leaky but there is an increase in area. However, we employ SG FinFET than the other two types in designing CAM as it is superior in terms of delay and area.

Cam Review

In this section, operation of the CAM and an example of its use in routing is described.

Operation of CAM

Fig. 1 shows a simplified block diagram of a CAM. It consists of search data registers, encoder, match lines, lookup table. The input data is given to the search lines which are connected to the lookup table. All the matched lines are pre-charged to High level. The CAM bit cell compares the input bit with the stored bit. Match lines with all bits matched maintain in the pre-charged high state. Match lines in which at least one bit mismatch, discharges to ground.

The match lines are given to an encoder that generates the match location corresponding to the match line that is in the high state. A simple encoder is used if only one match is probable. Some CAM applications will produce more than one word as match. In such cases, a priority encoder is used instead of simple encoder.

Example

An example of operation of CAM in Network routers is shown in Fig.2.The router has a routing table like TABLE I that has four entries. The "X" in the table denotes the "don't care" which means X may be 0 or 1.For example, if router obtains a packet with destination address 10010, the packet is forwarded to port A. Suppose if packet with destination address 1101X is given to router, then both entry 3 and 4 matches in the lookup table. But, entry 3 is selected, since it has less X bits. The entry 3 is encoded to match location 10.This match location 10 is given as input address to RAM.RAM which contains a list of ports, outputs port 3 corresponding to input address 10. Then the packet is forwarded to port 3.

Table I Example Routing Table

Entry No	Address(binary)	Output Port
1	100XX	A
2	1010X	B
3	1101X	C
4	110XX	D

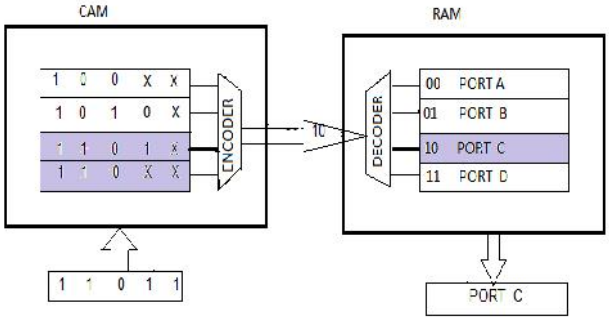


Fig2 Cam Based Implementation Of Routing Table I

Design of Finfet Cam

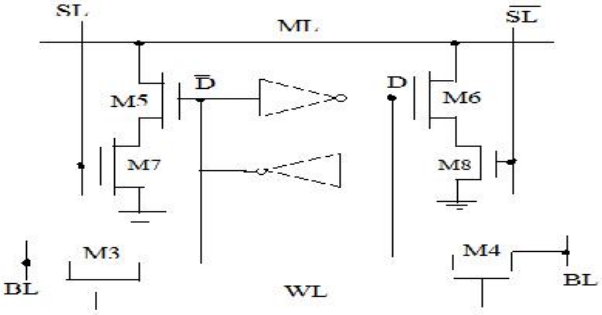
In the architecture of CAM, the major part is CAM bit cells. In this paper, such a CAM bit cell is designed using Shorted Gate type FinFETs.

CAM cell Circuits

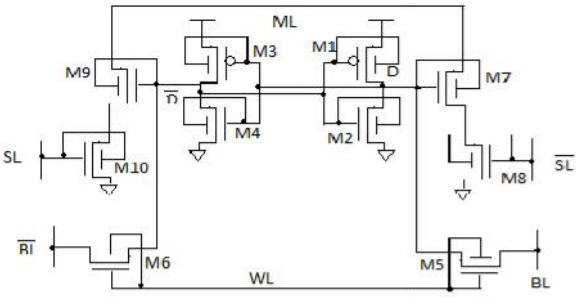
Each CAM bit cell contains two parts: a storage unit and a comparison circuitry. The storage unit is the one in which data is stored. The comparison circuit is to compare whether the search data is matched with stored data. Two types of CAM cells are used in most of the CAMs: Binary CAM cell (BCAM) and Ternary CAM cell (TCAM). The BCAM cell is made of 6-9 transistors, while TCAM cell requires 12-17 transistors in standard CMOS design. Since the die area of TCAM is larger than the BCAM, BCAM is mostly preferred.

Proposed CAM using SG FinFETs

In this paper, we propose BCAM NOR cell using ten transistors. The storage unit is made of a typical 6T SRAM cell. The comparison unit is made of XOR/XNOR matching circuitry for data comparision.CAM can be classified into NOR, NAND categories. The NOR CAM bit cell using conventional MOSFET, as shown in Fig. 3(a), has cross coupled inverters and transistors M3 and M4 that forms the storage unit, while M5-M8 transistors form the comparison unit.



(a) Using conventional MOSFET



(b) Using SG FinFET
Fig3 Schematic diagram of NOR CAM bit cell

In the proposed diagram as shown in Fig. 3(b), the same NOR BCAM bit cell is designed using SG type FinFET. In that Fig. 3(b), M1–M6 forms the core SRAM cell, while transistors M7–M10 form the matching circuit.

The Schematic of proposed NOR CAM bit cell is simulated in 22nm technology. The design parameters and two dimensional cross-section of 3D-FinFET are given in TABLE II and Fig.4 respectively.

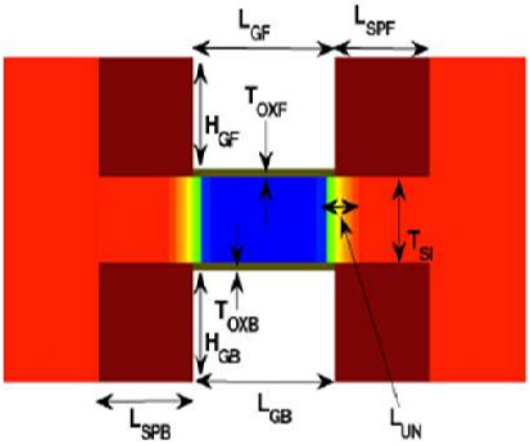


Fig4 2D cross section of 3D FinFET

Table II 22-Nm Finfet Device Parameters

L_{GF} , L_{GB}(nm)	24
Effective T_{OXF} ,T_{OXB}(nm)	1
T_{SI}(nm)	10
H_{GF}, H_{GB}(nm)	10
L_{SPF}, L_{SPB}(nm)	12
L_{UN}(nm)	4

EXPERIMENTAL RESULTS

The proposed NOR CAM bit cell can be designed in TANNER EDA tool in 22nm technology. The CAM design shown in Fig.3 (b) is drawn in S-Edit (Schematic Editor) of Tanner EDA as shown in Fig.5. While designing, the 22nm parameters of FinFET given in TABLE II are used. Then, the circuit is simulated and the output waveforms of select line (SL, $\overline{SL}$), match line (ML, $\overline{ML}$) and bit lines (BL, $\overline{BL}$) are viewed in Waveform Editor, W-Edit as shown in Fig.6. Then, the average power consumed, maximum power, minimum power is obtained from T-spice as shown in Fig.7 and the results are compared with conventional MOSFET in TABLE III.

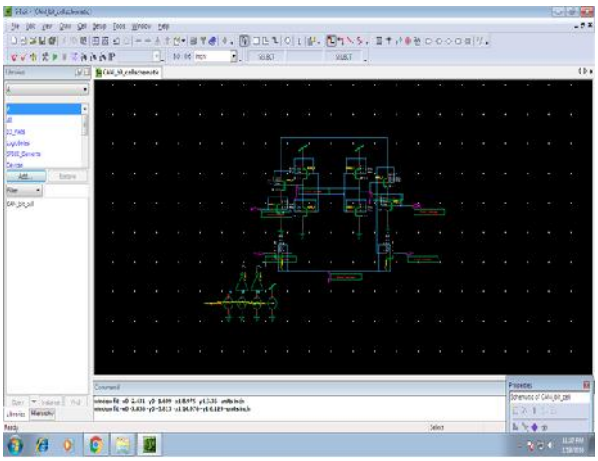


Fig.5 Schematic of NOR CAM bit cell using SG FinFET in S-Edit Tool

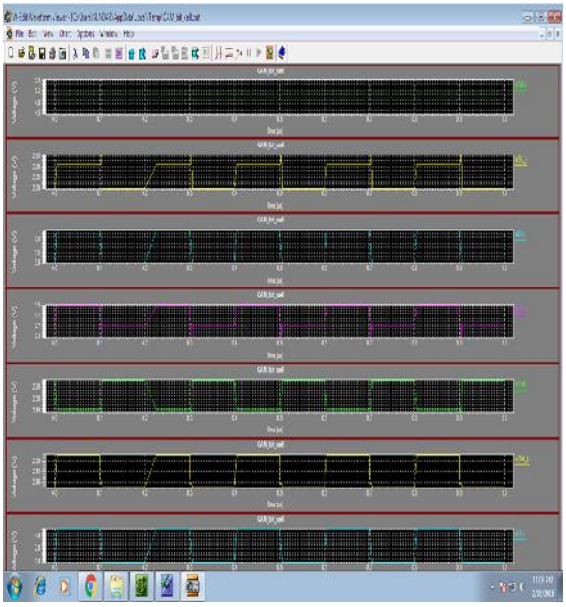


Fig.6 Output Waveforms of the NOR CAM bit cell in the W-Edit Waveform viewer

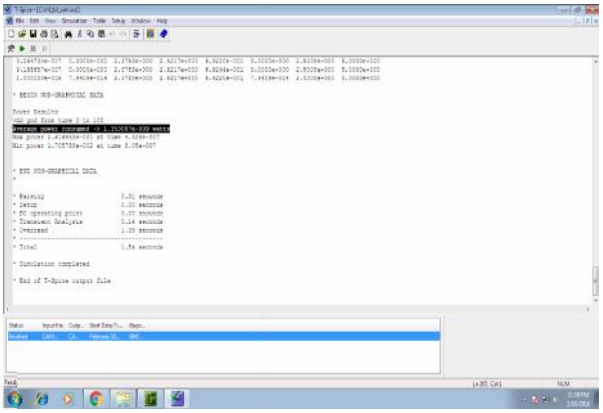


Fig.7 Report of the Schematic in T-Spice

Table III

Parameter	CAM cell using MOSFET	CAM cell using FinFET
Average power consumed	1.898992e-007 watts	1.353097e-009 watts

Thus, the average power consumed is 1.353097e-009 watt which is very less compared to the one using MOSFET.

CONCLUSION

The most important consideration in designing a device is less power dissipation and high performance. In this paper, we proposed a new design of NOR content addressable memory using Shorted Gate FinFET, instead of conventional MOSFET. Because of replacing MOSFET by FinFET, the power consumption is reduced from $1.89x10^{-7}$ watts to $1.35x10^{-9}$ watts. Thus, by using FinFET, power efficient devices can be designed.

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How to cite this article:

Dineshkumar T.R *et al*.2016, Design of Nor Content Addressable Memory Bit Cell Using Shorted Gate Finfets. *Int J Recent Sci Res.* 7(2), pp. 9071-9074.

TSSN 0976-3031