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RESEARCH ARTICLE

PERFORMANCE ANALYSIS OF LOW POWER HIGH SPEED CARRY SELECT ADDER

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ABSTRACT

Adder plays a major role in any part of the combinational system like subtractions, high speed multiplication, DSPs and ALUs. Any computational system requires fast process to be carried out. Carry select adder (CSLA) is one of the high speed adder used in many computations to perform fast arithmetic operations. The logic operation involved in conventional carry select adder and binary to excess -1 converter based CSLA are analyzed to study the data dependence to identify redundant logic operations. The modified CSLA has been developed using gate-level modification to significantly reduce the delay and power of CSLA. Based on this modification 8-,16-,32-,64-,and 128-bit square root carry select adder(SQRT CSLA) architecture have been developed and compared with regular carry select adder architecture. The proposed design for higher adder has reduced power and delay is compared with the regular and modified SQRT CSLA. For 256-bit addition, it is proposed to simple gate level modification which significantly reduces the power by 19.4%. So this paper specially concentrates on speed and area constraints of CSLA.

INTRODUCTION

In recent years, the increasing demand for high-speed arithmetic units in micro-processors, image processing units and DSP chips has paved the path for development of high-speed adders as addition is an indispensable operation in almost every arithmetic unit.It also acts as the basic building block for synthesis of all other arithmetic computations. To increase portability of systems and battery life, area and power are the critical factors of concern. Furthermore for the applications such as the RISC processor design, where single cycle execution of instructions is the key measure of performance of the circuits, use of an efficient adder circuit becomes necessary, to realize efficient system performance. However the regular-csla is not area and power efficient because it uses multiple pairs of ripple carry in order to generate a partial sum with Cin=0 and Cin=1,then the final sum and carry are selected by multiplexers.

The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption . The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure.

Design of area-efficient and power-efficient high-speed logic systems is one of the crucial areas of research in VLSI design. The major speed limitation of adders arises from the huge carry propagation delay encountered in the conventional adder circuit, such as RCA and carry save adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position.

Delay Evaluation Methodology of the Basic Adder Blocks: The AND, OR, and Inverter (AOI) are used for the implementation of an XOR gate. The numeric representation of

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each gate indicates the delay contributed by that gate. The delay evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. We then add up the number of gates in the longest path (worst path) of a logic block that contributes to the maximum delay.

Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I.

Table I

Adder Block	Delay
XOR	3
2:1 Mux	3
Half Adder	3
Full Adder	6
BEC-1	2

MATERIALS

The main idea of this work is to use BEC instead of the RCA with Cin = 1 in order to reduce the area and power consumption of the regular CSLA. To replace the *n*-bit RCA, an *n*+1-bit BEC is required. The modified CSLA architecture has developed using Binary to Excess-1 converter (BEC). Fig. 1 illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. The XOR gate in BEC of Modified CSLA is replaced with the optimized XOR gate in AOI of Modified Area Efficient CSLA .With BEC there is reduction of gates by replacing n bit RCA with n+1 bit BEC .When the optimized XOR gate is used in Modified CSLA, it is verified that there is large reduction in number of gates. The MUX is used to select either the BEC output or the inputs given directly to a BEC circuit of next block. In this design, the major function of MUX is to derive the adder speed.

According to the control signal Cin, the mux is used to select the output from the inputs (input bits as per the block size and the BEC output). The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols ~ NOT, & AND, ^ XOR)

X0 = ~B0
X1 = B0 ^ B1
X2 = B2 ^ (B0&B1)
X3 = B3 ^ (B0&B1&B2)

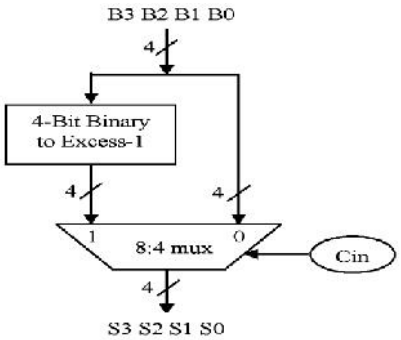


Fig. 1 BEC with mux

METHODS

Regular SQRT carry select adder

A sqrt carry select adder is constructed using the conventional 4-bit ripple carry adder (RCA). The RCA uses multiple full adders to perform addition operation. Each full adder inputs a carry-in, which is the carry-out of the preceding adder. The CSA divides the words to be added into blocks and forms two sums for each block in parallel, one with assumed carry in (Cin) of 0 and the other with Cin of 1. The carry-out from one stage of 4-bit RCA is used as the select signal for the multiplexer. This selects the corresponding sum bit from the next block. This speeds up the computation process of the adder. Thus, the carry select adder achieves higher speed of operation at the cost of increased number of devices used in the circuit. This in turn increases the area and power consumed by the circuits of this type of structure.

Delay Evaluation Methodology of Regular 16-b Sqrt

CSLA: The structure of the 32-b regular SQRT CSLA is shown in Fig. 2. It has groups of different sizes RCA.

1. The group2 [see Fig. 3(a)] has two sets of 2-b RCA. The sum3 is summation of S3 and mux and sum2 is summation of c1 and mux, based on the delay values stated earlier and thereby their respective arrival time.
2. Except for group2, the arrival time of mux selection input is always greater than the arrival time

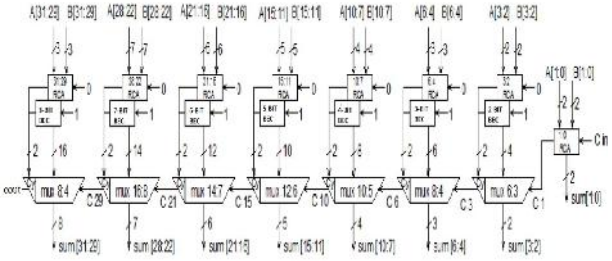
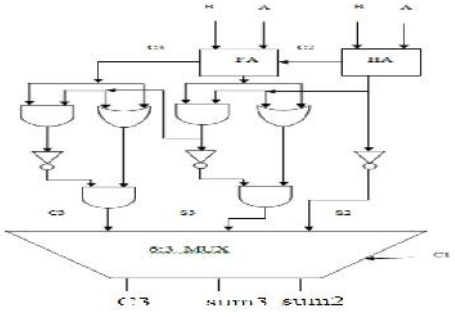


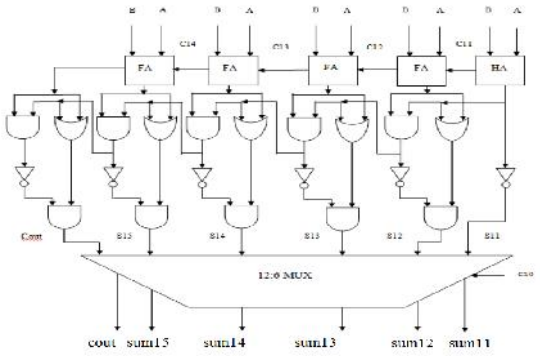
Fig. 2 Modified 32-b SQRT CSLA

of data outputs from the RCAs. Thus, the delay of other groups is determined, respectively as follows:

c6, sum[6:4]} = c3[t = 10] + mux
c10, sum[10:7]} = c6[t = 13] + mux
c15, sum[15:11]} = c10[t = 16] + mux



(a)



(b)

Fig. 3(a) group 1 (b) group 5 (Modified CSLA)

Proposed Sqrt Carry Select Adder

In this type of Adder, the block of Ripple Carry Adder with input carry as 1 has been replaced with a block of Binary to Excess-1 converter (BEC) as shown in fig 2. This is done in order to reduce the area and power requirement of the previous conventional Carry Select Adder. The maximum estimated areas of each group of the modified and regular SQRT CSLA are given in table II.

Table II (Area count of CSLA)

Group no.	Regular	Modified
2	64	50
3	94	73
4	124	96
5	154	119
6	184	142
7	214	165

Table III (% Reduction)

Word size(bit)	Area	Area-Delay	Power	Power-delay
8	17.3	5.5	12.10	0.46
16	19.02	10.3	13.81	4.34
32	20.2	13.2	16.87	8.41
64	20.69	18.1	17.84	15.05
128	20.8	19.5	18.78	17.4
256	21.58	22.28	19.4	21.1

The Percentage reduction of CSLA for different word sizes are given in table III.

Delay Evalution methodology Of Modified

32-b SQRT CSLA: The structure is given in fig. 2. The steps leading to the delay evaluation are given here table 1 and table 3.

1. The second group has a 2-b RCA. Instead of another 2-b RCA with Cin = 1 a 3-b BEC is used which adds 1 to the output from 2-b RCA. Based on the values of Table I, the arrival time of selection input c1 of 6:3 mux is earlier than the s3 and c3 and later than the s2. Thus, the sum3 and final c3 (output from mux) depend on s3 and mux and partial c3 (input to mux) and mux, respectively.
2. For the remaining groups the arrival time of mux selection input is always greater than the arrival time of data inputs from the BECs. Thus, the delay of the remaining groups depends on the arrival time of mux selection input and the mux delay.

Comparing the delay values of the earlier models and the proposed model, the reduction in area, power and delay values are given in table IV. percentage

RESULTS AND DISCUSSIONS

The design proposed in this paper has been developed using Verilog- HDL and synthesized in Cadence RTL compiler using typical libraries of TMSC 180nm technology. Designs of CSLA were developed using structural Verilog module and synthesized using Xilinx ISE simulator, version 10.1 and the implementation is done in cadence RTL compiler.

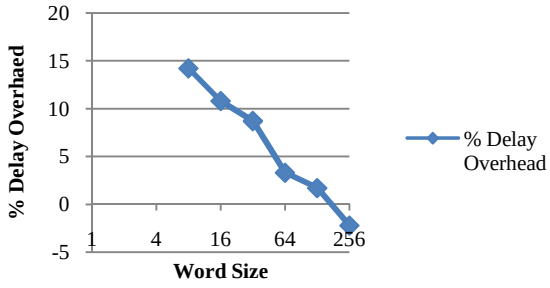


Fig. 4 Percentage of delay overhead.

Table IV Implementation Result

Word Size	CSLA	Delay(ns)	Area(um^2)	Power(µw)			Power-delay product (10^{-15})	Area-Delay Product (10^{-21})
				Leakage Power	Switching Power	Total Power*		
8-bit	Regular	0.700	1134	0.043	96.021	96.065	67.2455	793.8
	Modified	0.800	0938	0.034	84.411	84.446	67.5568	750.4
16-bit	Regular	1.212	2472	0.095	226.311	226.407	274.4052	2996.06
	Modified	1.343	2002	0.070	195.305	195.37	260.518	2688.56
32-bit	Regular	1.926	5246	0.199	504.093	504.293	971.268	10103.79
	Modified	2.095	4188	0.152	424.497	424.649	889.639	8773.86
64-bit	Regular	3.500	10694	0.407	997.391	997.798	3492.293	37429.0
	Modified	3.616	8482	0.307	820.153	820.461	2966.798	30670.91
128-bit	Regular	5.644	21961	0.826	2176.423	2177.249	12279.63	123860.0
	Modified	5.736	17394	0.634	1837.932	1768.567	10144.505	99771.98
256-bit	Regular	9.804	44684	1.672	4546.005	4547.678	44588.435	438081.9
	Modified	9.598	35044	1.253	3665.546	3666.800	35193.949	336352.3

*Total Power=Leakage Power + Internal Power + Switching Power

The percentage reduction in the total power dissipation and the delay, with respect to the worst path of the flow is given in table III. The analysis shows that there has been a considerable decrease in the power and delay with slight increase in the area compared to the earlier work B.Ramkumar *et al*(2012) .The implementation results are as shown in table IV. The percentage of delay overhead is as shown in fig.4 and the percentage reduction in the cell area, total power, power-delay product and the area–delay product as function of the bit size are shown in Fig. 5.

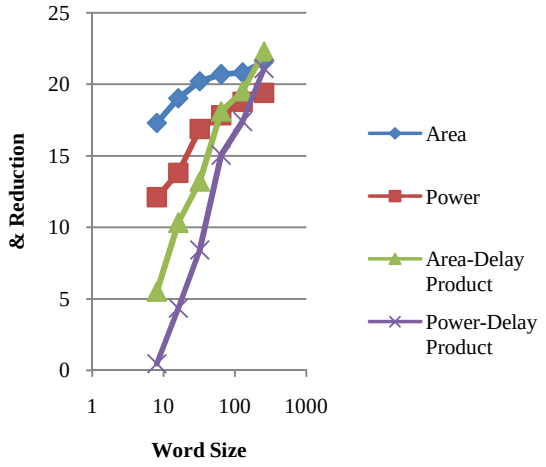


Fig. 5 Percentage reduction in the cell area, total power, power–delay product, and area–delay product.

CONCLUSION

After comparing the different parameters of various adders with the proposed modified SQRT CSLA, it is evident that the power dissipation has been reduced to the desired extent with a slight increase in area. The proposed model provides a good tradeoff between the time and power consumption. Hence the modified 256-bit CSLA is more efficient for the VLSI hardware implementation. Further work is to be done in reducing the area and for higher order adders (512-bit), thus improving the overall system performance as such.

References

Bedrij O.J 1962 Carry-select adder *IRE Trans. Electron. Comput.*, pp.340–344.

Moris Mano M 2002, Digital Design Pearson Education, 3rd edition

Ramkumar.B and Harish M Kittur 2012, Low-Power and Area-Efficient Carry Select Adder, *IEEE on VLSI System vol.20 No.2*

Ramkumar.B ,Harish M Kittur and Kannan P M 2010 ASIC implementation of modified faster carry save adder, *Eur. J. Sci. Res.*, vol. 42, no. 1, pp. 53–58

Rabaey J M 2001 Digtal Integrated Circuits—A Design Perspective Upper Saddle River, NJ: Prentice-Hall

Kim Y and Kim L-S 2001 64-bit carry-select adder with reduced area, *Electron. Lett.*, vol. 37, no. 10, pp. 614–615

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