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Research Article

IMPLEMENTATION OF LOW POWER D-FLIPFLOP USING 45NM CMOS TECHNOLOGY

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ABSTRACT

Designing low power devices is now a major sector of research due to increased demand for portable devices. Because MOS devices are widespread, there is a great need for less energy-consuming circuits, especially for portable devices and laptops. A memory element consumes 70 percent of total power in an integrated circuit. As flip-flops are the main area of memory elements used on any portable device, the major concern to reduce flip-flop energy consumption will help reduce power consumption in an IC considerably. In this paper we designed a flip-flop using CMOS logic; it consumes less energy than conventional gates designed. Transistors switching occurs when input and clock is applied. We proposed clocked D flip-flop, transient 0.7V power supply dissipation analysis and various applications of D flip-flop. This flip-flop is implemented using 45 nm Technology in virtuoso cadence.

INTRODUCTION

Sequential circuits are logic circuit whose output in any occurrence of the time depends not only on current input but emits past. Sequential circuits are of two types: (i) clocked and (ii) unclocked. The simplest type of sequential circuit is a memory cell with two states. It can be 1 or 0. These two state circuits are called sequential flip-flop, as it moves from one state to another and then fall back.

Flip-flops are used as memory elements which are the basic elements of an integrated circuit. They are used in many applications such as data storage registers in parallel flow, counter and frequency division, etc....Computers and calculators machines utilize Flip-flop for their memories. A combination of the number of flip flops can produce a certain amount of memory.

Flip-flop is built using logic gate, which in turn is made of transistors. Flip-flops are the basic building blocks of electronic memory devices. Each flip-flop can store a piece of data.

It have two stable states, and therefore, Multivibrators flip-flop. Both stable states are high. The term flip-flop is used as switchable between states under the influence of a control signal (clock or active), for example, the state you can "flip" and "flop" back to another state. In this proposed work we designed the inverted D flip-flop by transistor level circuit.

Working of D-Flip Flop

The D flip-flop is commonly used. This is also known as a "data" or "delay" flip-flop. When applied without a clock input on the D flip-flop or the falling edge of the clock signal, there will be no change in output. Keep the previous output value Q and inverts for Q'. If the clock signal is high (rising edge is more accurate) and D input is high, the output Q is high, the output Q' is low and where D input is low, the output Q will be

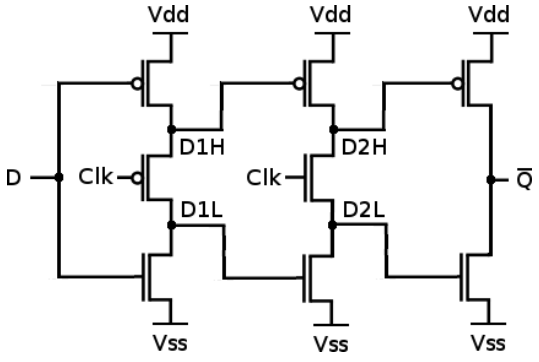

Figure 1 D flip-flopimplementation using transistor level logic

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low, the output Q' is high. Therefore, the output Q follows input D and Q' follows the invert of Q in the presence of a clock signal.

Table 1 D Flip-flop truth table

Clock	D	Q	Q'
0	X	LAST STATE	LAST STATE
1	0	0	1
1	1	1	0

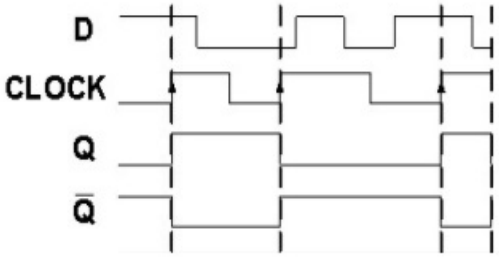
If D = 0; Q = 0; Q' = 1 so flip flop is reset.
If D = 1; Q = 1; Q' = 0 so flip flop is set.

Operation

Operation of positive edge triggered Master Slave D flip flop is explained below.

If the clock is low, the signal to allow the master flip-flop is high. When the clock signal changes from low to high, master flip-flop data will store from input D. At the same time, the second flip-flop enable signal goes from low to high with clock signal due to double inversion. Data blocked flip-flop master during the rising edge was sent slave flip-flop.

When the clock signal goes from high to low, exit master-slave flip-flop Flip failure as input and change their state. Master Memory Element supports the latest input values in the next rising edge.



Graph 1 Timing Diagram of D Flip Flop

Applications

D flip-flop is one of the most widely used. Some of the many D-flip-flop applications-

1. Data storage registers.
2. Data transferring as shift registers.
3. Frequency division circuits.

Data Storage

Normally data of digital circuits is stored as a bunch of bits, represented by numbers and codes. Therefore, it is easy to create and store data in parallel data lines simultaneously with a group of flip-flops arranged in a specific order. Registers are based on data from multi-bit devices. These are generated by linking the number of D flip-flop, in order to be able to store more bits of data.

Each D flip-flop input is connected to the data. Input clock is applied the same for all flip-flop, to apply all data simultaneously from their D inputs when a clock signal triggers a positive edge.

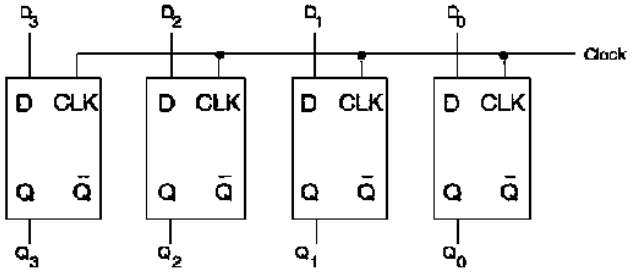


Figure 2 D Flip-flop arranged to store data in parallel

Data Transfer

D flip-flop is also widely used in data transfer. To transfer data D Flip - Flop is connected to generate a shift register. A cascade connection of D flip-flop with the same clock signal to generate a shift register. A shift register can change the data without changing the order of the bits. When applying a clock pulse, one bit of data is moved or transferred. The shift register can store data temporarily.

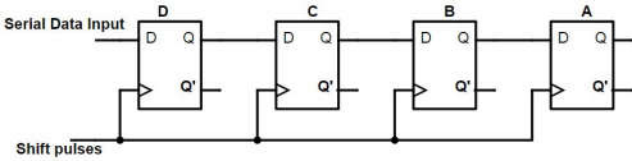


Figure 3 4-Bit shift register using the D flip-flop

The shift register used in serial to parallel conversion and parallel to serial conversion of data set. They are also used to extend pulse and as delay circuits.

D Flip Flop Using as Frequency Division

Circuit's frequency division is developed using D flip-flop. This is one of the most important applications of Flip Flop D. The frequency division circuit, the state of flip-flop output (Q ') is connected to input of data (D) as a feedback loop. Two successive pulses of the flip-flop will cause toggle, for every two cycles of clock.

As the name suggests, frequency divider circuits are used to generate digital output signals exactly half of the input frequency. Circuit's frequency dividers are basically used in the design of asynchronous counters.

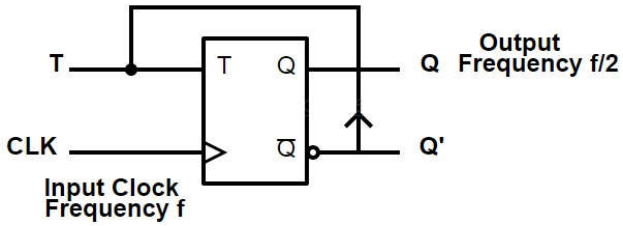
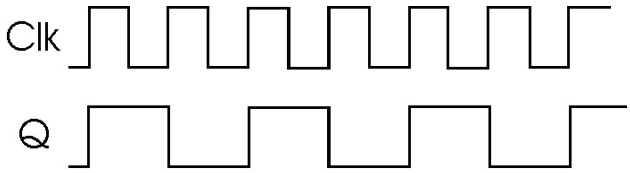


Figure 4 Frequency divider circuit of D Flip-flop

The operation of the circuit is very simple. The incoming data signal is clocked by the clock input signal. The circuit will perform the division of the input frequency by using the feedback loop i.e. connected to the Data input from Q'. The frequency divider circuit divides the input frequency by 2 for every two clock pulses.

Circuit operation is very simple. The input signal is synchronized with the clock input. The circuit will perform

frequency division input with a circuit feedback which is connected to input from output (Q'). "Frequency divider circuit divides the input frequency by 2 for each two clock pulses.



Graph 2 Graph of frequency divider D Flip-flop circuit

This can be explained with respect to the output of the clock signal.

In a situation where the Q output is 1, the Q' output is 0, the input data is synchronized from the Q output of D to the next rising edge of the input signal clock. In this case the variation of the output high to low occurs. This output remains unchanged until the occurrence of the next positive clock signal. Similarly, the output (Q') is also synchronized. As the clock input is 1 again, it will change the status of output flip-flop.

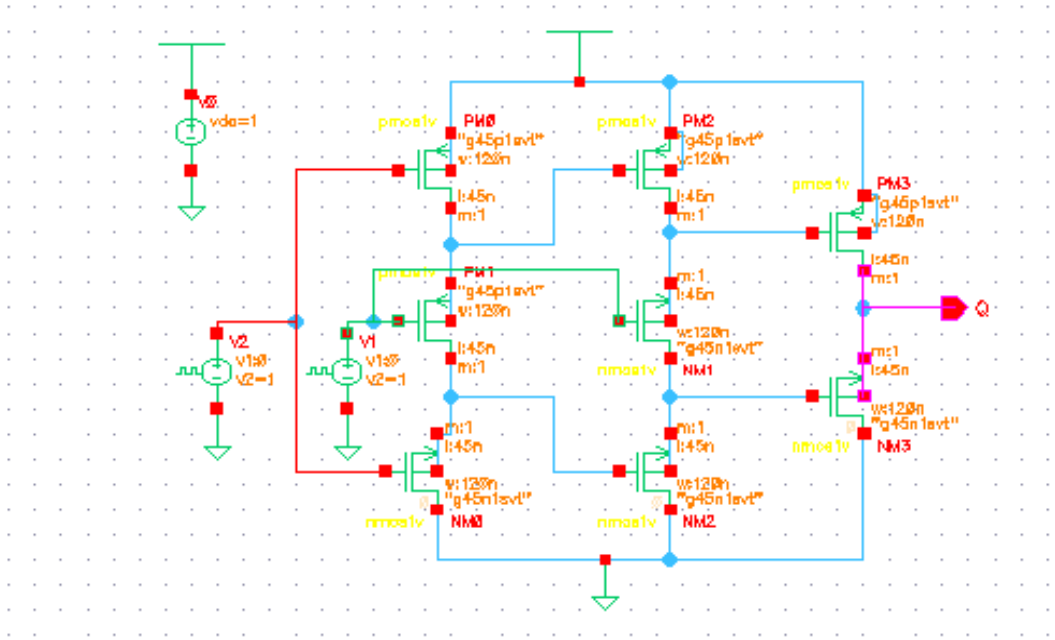
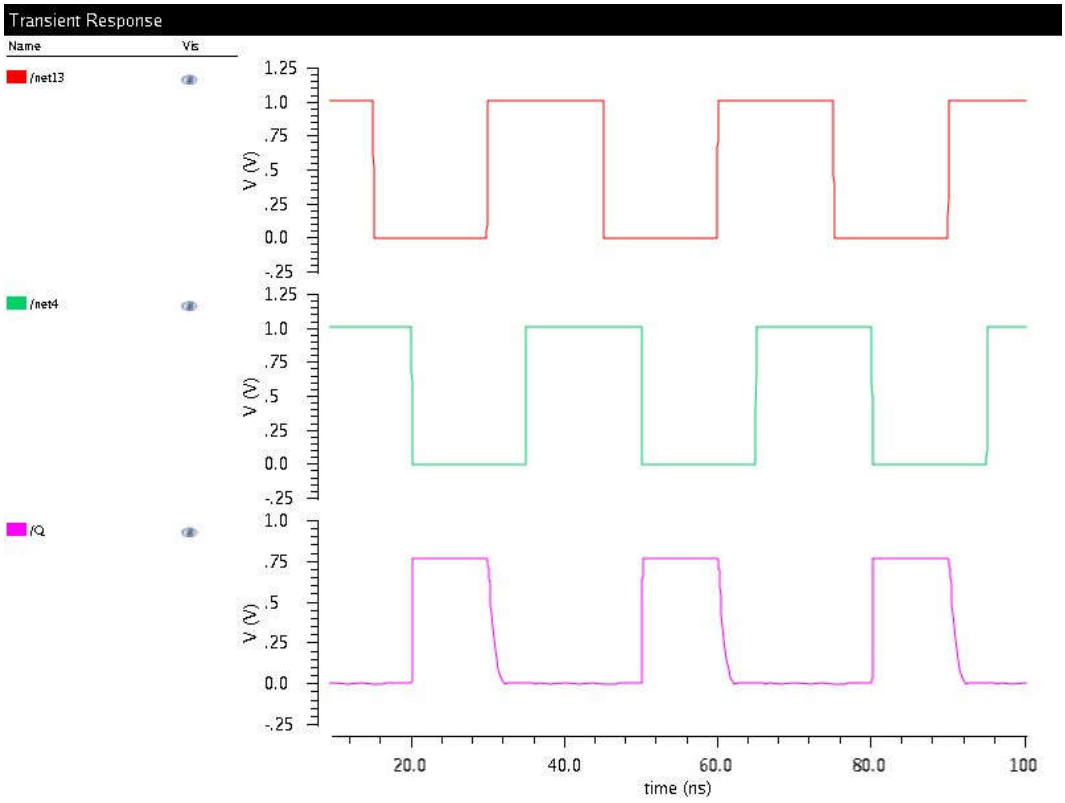


Figure 5 Transistor level logic of D Flip-flop using 45nm technology



Graph 3 The Transient Response of D flip flop.

We can see that the output of the frequency divider circuit changes only the input of the clock signal marginally positive. We know that every positive edge occurs once in a clock cycle. So, depending on the positive edge of the D flip-flop clock is half the pulse input, which divides 2 clock pulses.

Stimulated Results

As we designed D Flip-Flop by transistor level logic for saving of energy as compare to the combinational design and more accurate working response compare to other technologies. We implemented this circuit in 45n technology.

Here we consider Q as Q' in the below figure

Advantages of D- Flip Flop

- Flip-flops are binary storage devices that can store binary data (0 or 1).
- Flip-flops are edge sensitive devices or triggered by edges, which are sensitive to the switch, rather than the duration or width of the clock signal.
- They are also known as sensors to signal changes, that is, fix the clock signal makes the difference in the flip-flop production.
- A bistable operation according to clock pulses.
- The pistons are also used to control the functionality of the digital circuit. They can change the operation of a digital circuit, depending on the state.
- D flip flops are also used in finite state machines.

CONCLUSION

In this paper, D flip-flop has been implemented using more number of Transistor. With low-power applications, the area and power consumption of the device are the key technological aspects to prefer a drawing to other models. Fully personalized drawing set D flip-flop shows better performance in terms of power dissipation and the area of the illustrations described in this paper.

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