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Research Article

TAPERING INTERCONNECT TOPOLOGY FOR HIGH SPEED VLSI DESIGN

Darshan Halliyavar[1] and Srividya P[2]

[1]VLSI Design and Embedded Systems RV College of Engineering, Bengaluru
[2]Department of ECE RV College of Engineering, Bengaluru

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ABSTRACT

Optimizing the interconnects plays an important role in core CPU architecture to obtain higher speeds. Interconnects consists of RC components, for which decreasing the RC delay plays an Important role. There are many Interconnect topologies but the optimal one helps in obtaining the minimal delay. The paper explains a new interconnect routing technique called Tapering to reduce this delay. Tapering routing topology helps in getting the minimal RC delay. It uses the Elmore delay model to get the minimal RC delay. The right percentage of tapering will fetch optimal results. Further implementation of this topology can be automated and can be effective in improvising the speed. In this technique, the resistance near the driver is made higher and the capacitance near the receiver is lowered. This leads to the improvement in RC delay. At first, the routing is done manually for a small portion of the chip and subsequently it is automated to do the routing for the entire section of the chip. Using the technique, it is observed that RC delay decreases by 10% to 30%.

INTRODUCTION

The scaling of CMOS transistors has led to the improvement in device performance with increased transistor density and reduced power consumption. Scaling of interconnects plays an important role as it reduces the usage of area, power and also resolves the timing issues. To improve the delay aspects of interconnects one has to focus on improving the routing techniques. Thus for this purpose Tapering routing technique has been introduced in this paper to make it a high speed interconnect. This routing technique uses the concept of Elmore delay model which tells that increasing the width near the driver side and decreasing the width near the receiver side helps in decreasing the RC delay. It means that the value of the resistance has to be more near the driver side than that of the receiver side and the capacitance value is vice versa. Further this technique which is developed can also be proved mathematically.

This technique is first done manually for few nets and results are calculated. The design is then automated to test the entire chip with number of nets. By automation, the accuracy increases. Shielding is another technique of adding extra net which is connected to VDD or VSS. This helps in removing the effects of cross coupling capacitance in between the adjacent nets. Thus tapering technique with the combination of shielding i.e. half shielding and full shielding will lead to decrease of RC delay values. Least RC delay for a particular net is obtained by comparing the RC delays obtained for the net using some of the high speed routing techniques like metal strapping and shielding. Further the entire utility can be automated and all the topologies can be compared and tested to obtain the best results.

Previous Work

With the increase in the operating frequency, the VLSI interconnects becomes critical for the overall system design. There has been active research in optimizing interconnect delays and much progress has been made. Many interconnect models like ideal wire, lumped, distributed models are developed. These models help in modelling the interconnects easily.

In papers[1-4], performance modelling of high speed interconnects are developed and optimization of these interconnects are carried out. The papers also provide information about optimizing global wire widths. The different design objectives and wire length distributions as suggested in the papers can be considered during wire width planning. However, these methods have small amount of errors compared

Corresponding author:* **Darshan Halliyavar
VLSI Design and Embedded Systems RV College of Engineering, Bengaluru

with the optimal solutions. Thus the inference from these papers is that the simplified wire sizing schemes and wire width planning methodology will be very useful for better design convergence and simpler routing architectures.

Paper [8] describes the modelling and simulation of tapered nets for clock distribution networks which helps in reducing the delay. In addition to this the tapering can be done for the ground wires and delay can be obtained. To improve the RC delay of the nets some of the techniques like metal upgradation to higher layers, strapping, widening, shielding can also be done. Some of these techniques are implemented to resolve issues concerned with area, timing and availability of resources. Since interconnect has become a dominant issue in high performance ICs, the focus of the circuit design has been shifted more towards interconnects optimization. An improvement of RC delay was achieved with the help of different combinations of higher layer metals which are of less resistance. Multiple criteria such as delay, power dissipation, noise, bandwidth, and physical area was considered during the interconnect design process.

Tapering techniques

The Elmore delay model, plays an important and huge role in reducing the RC delay. This model cannot be applied to tapering wire technique practically because the wire width at the receiver side and driver side cannot be different. So a new topology is proposed in which double routing is done near driver side and single track routing is done near the receiver side. The conventional and new wire topology are shown in the Figure1 and Figure 2 respectively.

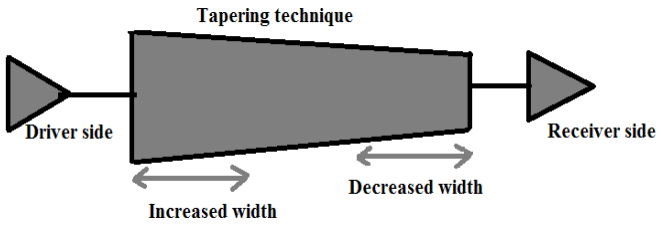

Figure 1 General Tapering technique.

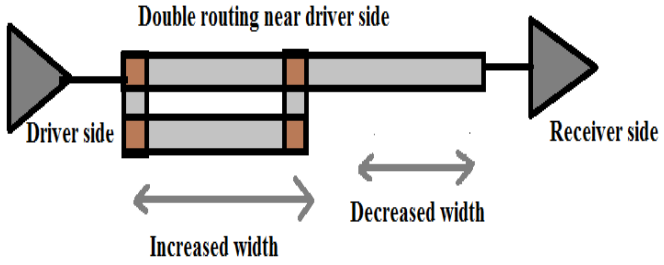

Figure 2 New Tapering Technique

In the proposed new technique, double routing is done near the driver side with tapering of 10% to 50% and end to end simulation results are observed. Tapering percentage plays an important role in RC delay. If tapering percentage increases more than 50% it is observed that there is no eventual decreases in the RC delay. There are chances that it might even lead to increase in RC delay. So the right percentage of tapering should be done. The combination of metal layers also plays a very important role in deciding the RC delay.

METHODOLOGY

Using custom tools manual implementation of routing is done for some of the nets. An algorithm is developed for automatic tapering technique with their respective set of metal and via attributes. Further the DRC cleaning is done. The DRC cleaning is done manually for each net with help of ICC tool. The tool follows a certain design rule to draw the layout. Thus violations are checked after routing. Some of the issues like via to via, minimum length, shorts, spacing, etc. have to be cleaned. If DRC violations are not cleaned there will be no visible improvement in RC delay. So preventive measures have to be taken to check the DRC violations. Figures 3 and 4 shows the implementation of tapering routing technique done through the ICC tools by manually and automation respectively.

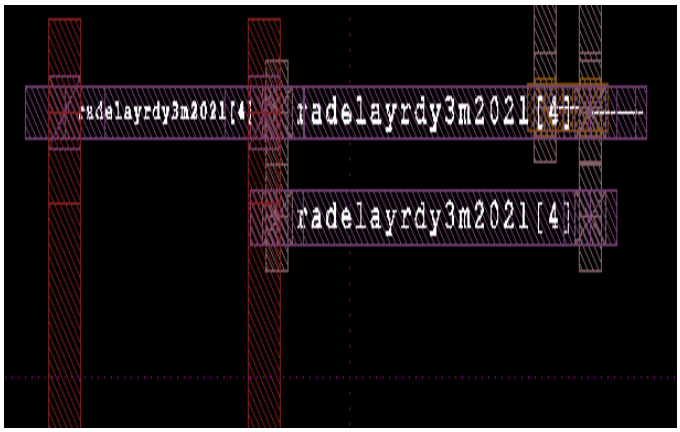

Figure 3 Tapering of the net done manually.

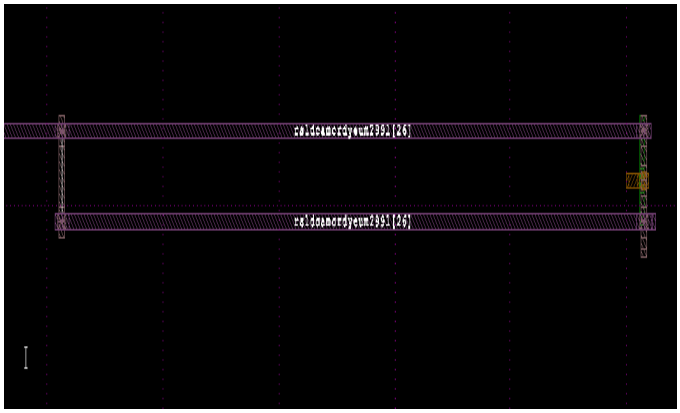

Figure 4 Tapering of the net done through automation

Automatic routing algorithm for tapering technique:

- The algorithm finds the x, y coordinates and the metal layer on which the tapering has to be done.
- If the metal layer for which tapering is to be done is small, then it does not proceed further as there will be no considerable improvement in the RC delay.
- The routing technique is not done to clock net and power nets.
- It checks for the empty space beside the track so that the extra routing can be done easily.
- The extra routing technique is done and via's are placed correctly for the respective metal attributes.
- The procedure is written for cleaning the DRC violations and also checked if any DRC violations are found in the section.

- Then using the IC advisory, the RC delay value is calculated for both the tapered nets and that of non-tapered nets.
- A code is written for the comparison of the both the delay files which are obtained through the IC advisory.

RESULTS AND DISCUSSION

The RC delay of the nets are noted before and after tapering and the difference between the nets are calculated and the percentage improvement are tabulated in Table.1 .

Table 1 Results of 10 nets and their improvement in percentage

#Net	RC delay before tapering(ps)	after tapering (ps)	improvement in %
rseudepmatcheum203h[4][44]	0.0197	0.0175	11.16
aleubundselm201l[4][2]	0.014	0.012	14.28
rseudepmatcheum203h[4][42]	0.017	0.012	29.41
rseudepmatcheum203h[4][54]	0.028	0.023	17.85
aldispport5m201h[3]	0.027	0.02	25.95
rseudepmatcheum203h[4][46]	0.032	0.028	12.5
ooovrpt27e1idlsrcm200h#[1][2]	0.03	0.026	13.33
rseudepmatcheum203h[4][58]	0.023	0.02	13
ooovrpt49e1rsuopcvrm301h[5]	0.025	0.021	16

s

For simplicity, only the 10 nets are shown. The RC delay before tapering and after tapering is calculated through the IC advisory which is in picoseconds and the percentage improvement is tabulated in the last column in Table 1.

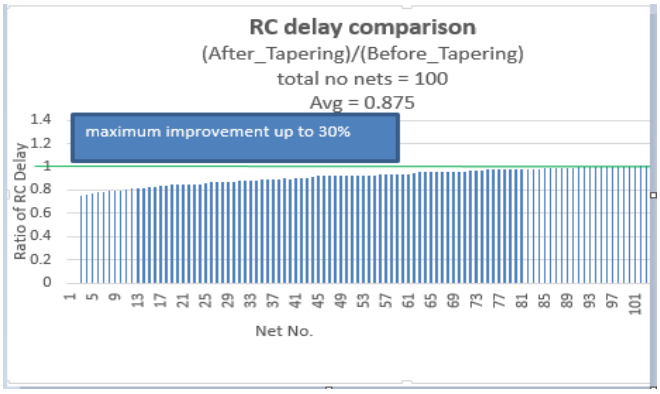

Figure 5 Graph showing RC delay comparison

Figure 5 shows the RC delay comparison of 100 nets of a particular section in a chip. The RC delay that is calculated before and after tapering are plotted to find the improvement in the ratio of RC delay. The RC delay ratio of more than 1 is considered as a worst case, so 1 is considered as demarcation line. Further a maximum decrease of up to 30% is observed in RC delay when compared with the original one. An average value of RC delay ratio is of 0.875.

CONCLUSION

The work presented in this paper suggests that double routing tapering technique proves effective in decreasing the RC delay. The RC delay decreases by 10% to 30% compared to the original one. Thus this routing technique is suitable for the high speed designs where speed plays a very critical role.

As a future improvement, this routing technique can be also be implemented for the nets having multiple fanouts. Further with several routing techniques a framework can be devloped which automatically helps us to know the better RC delay values.

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