ResearchArticle

A SECURE DATA TRANSMISSION BETWEEN CDMA TRANSMITTER AND RECEIVER USING PARAMETERISED WALSH SEQUENCES WITH SPEED & POWER ANALYSIS

Akshay M. Ahirkar* andShrikant S. Chamlate

Department of Electronics and Communication Engineering, K.I.T.S Ramtek, Nagpur, India

ABSTRACT

We Design CDMA Transmitter & Receiver forSecure Transmission of Message Signal Between them Using Walsh Sequences. As Walsh Sequences is a Random Signal/High Frequency Carrier Signal which Generates by Walsh Sequence Generator. Walsh Sequence Generator generates a Serial In Serial Out Signal in Binary Form. And Further It Passes with Input Signal in Terms of Runtime Walsh Sequences. Walsh Sequence is also used for Error Detecting and Error Correcting Mechanism. It used For Secure andEfficiant Communication. If any Error Occure during Transmission, Walsh Sequence Troubleshoot and Correct it and Passes to those Receiver whichever Required. The Further investigation consider FPGA parameters like Speed and PowerDissipation..Here we design a system with less time delay so that Speed of Transmission System is more And Power Dissipation is little as Compared to Previous One. The Above Design is Implemented in VHDL Code.The Design found their uses in many popular applications like multiuser communications such as CDMA, WCDMA, VLSI Testing, Pattern Recognition as well as image and signal processing.

INTRODUCTION

Code Division Multiple Access (CDMA) is utilized as a multiple access procedure in telecommunications radio framework that can transport interactive media movement at high information rates. This has turned out on account of the different reasons which added to development in remote innovation. It Include the requirement for exceedingly dependable telecom network and most imperative and security against listening stealthily and cryptanalysts, anusage of the modest information network.Multicarrier code division multiple access (MC CDMA) is a strategy that joins the benefit of multi-bearer regulation with that of code division multiple access to offer solid high information rate downlink cell communication administrations. MC CDMA networks proposed for the fourth era (4G) framework that will be characterized by the capacity to incorporate heterogeneous networks, particularly radio portable networks and remote networks that offers access to all administrations, constantly and all around.. It is utilized, as it has ended up being superior to traditional CDMA networks, FDMA, and TDMA.Direct sequence (DS) CDMA is utilized as a part of the third-age versatile communication standard to give high limit and high transmission rate over regular plans. Here we are going to learn about the Walsh sequence and how we proposed a more secure Walsh sequence. Walsh-Hadamard bipolar spreading sequences can be used for channel separation in direct sequence code division multiple access (DS CDMA) system. They are easy to generate and orthogonal in case of perfect synchronization. However, the cross-correlation between two Walsh-Hadamard sequences can rise considerably in magnitude if there is a non-zero delay shift between them. Unfortunately, this is very often the case for up-link (mobile to base station) transmission, due to the differences in the corresponding propagation delays. As a result, significant multi-access interference (MAI) occurs which needs to be combated either by complicated multi-user detection algorithms, or reduction in bandwidth utilization.

One of the primary points of interest of CDMA is that dropouts happen just when the telephone is no less than twice as a long way from the base station. Another burden of this innovation, when contrasted with GSM is the absence of international meandering capacities. The capacity to redesign or change to another handset isn't simple with this innovation in light of the fact that the net benefit data for the telephone is put on the real telephone, not at all like GSM which utilizes SIM card for this. Each other hindrance is the restricted assortment of the handset

Corresponding author: **Akshay M. Ahirkar**
Department of Electronics and Communication Engineering, K.I.T.S Ramtek, Nagpur, India

in light of the fact that it exhibit the real portable organizations utilize GSM innovation.

An inspiration to attempt research chip away at Direct Sequence Code Division Multiple Access (DS-CDMA) communication frameworks depends on preferences that DS-CDMA has inborn property of better commotion resistance, regular pool of shared radio channels accessible to all users, wide bandwidth, higher framework limit, and enhanced administration quality, larger amount of protection, expanded security and higher throughput. The 3G and 4G portable framework is developing quick and will give significantly higher information rates as in Clarke and de Lamare (2011). It depends on the incorporation of existing remote communication frameworks with expanded frequency go and diminished cell range of the base station. The 3G and 4G communication will require particularly composed and scaled down fix reception apparatus to address bandwidth issues and power appraisals as clarified by HamadAmeen and WidadBinti Ismail (2011). The parallel preparing capacity of FPGA based Programmable Logic Devices (PLDs) makes them in a perfect world reasonable for baseband/Radio Frequency (RF) computerized signal handling in CDMA applications in Boukadourn et al (2005). The decision of CDMA depends on the way that apportioning channel assets utilizing spread spectrum systems have number of points of interest contrasted with Frequency Division Multiple Access (FDMA) or Time Division Multiple Access (TDMA) plots in Clarke and de Lamare (2011). The framework has the inborn property of better commotion insusceptibility and different points of interest. The signal preparing for communication frameworks is performed in present day times completely in the computerized area, which requires high throughput. Less complex and committed equipment circuits can just give the fast preparing capacity to meet these differentiating prerequisites, in Do and Feher (1996). Essentially there can be two standard gatherings of strategies, called serial and parallel systems, which are utilized regularly to reduce interference levels in CDMA. A novel procedure of equipment construct configuration executed in light of FPGA for CDMA versatile communications framework has higher speed with the low multifaceted nature included.

Message Signal is a Input Binary Signal & Can transmit 'N' no of Bits and it encoded with Walsh Sequences. At the Receiver End Further Walsh Sequence Generator is Used to Decode Transmitted Signal From Transmitter and Provide Message Signal to Receiver.In perspective of hazardous development in the quantity of digital cellular endorsers, specialist organizations are winding up progressively worried about the constrained limits of their current networks. This worry has prompted the arrangement of brilliant antenna frameworks all through real metropolitan cellular markets. These shrewd antenna frameworks have normally utilized multi beam innovations, which have been appeared, through broad examination, recreation, and experimentation, to give considerable performance upgrades in FDMA, TDMA and CDMA networks [5]. Multi beam designs for FDMA and TDMA frameworks give the straight-forward capacity of the smart antenna to be actualized as a non-intrusive extra or appliqué to a current cell site without significant adjustments or extraordinary interfaces [2]. This paper primarily focuses on utilization of brilliant antennas in versatile communications that upgrade the capacities of the portable and cellular framework for example, speedier piece rate, multi utilize interference, space division multiplexing (SDMA), increment in run, multipath relief, diminishment of mistakes due to multipath fading, best reasonableness of multi-transporter tweaks, for example, OFDMA. In this section, we are going to learn about the Walsh sequence and how we proposed a more secure Walsh sequence. Walsh-Hadamard bipolar spreading sequences can be used for channel separation in direct sequence code division multiple access (DS CDMA) systems, e.g. [3]. They are easy to generate, and orthogonal in the case of perfect synchronization. As a result, significant multi-access interference (MAI) [4] occurs which needs to be combated either by complicated multi-user detection algorithms [6], or reduction in bandwidth utilization. In addition to improving synchronization properties, scrambling also helps in reducing MAI.

MATERIALS AND METHOD

Transmitter and Receiver

In CDMA Transmitter and Receiver System, Where Input data can be send to input of Transmitter with addition of High frequency Carrier Signal as Walsh Sequence. After that it modulated in the transmitter and Gives Transmitter Output. This Transmitter Data Again applied to Input of Receiver With Addition of Walsh Sequences and Finally got Receiver Output. But this is not Output Signal, This Signal Passes to Comparator, After that Output Signal is Generated. Here Walsh Sequence Acts as a major Role for Transmission & Reception Process.

Here, For Modulation Process we use X-OR Logic for Data Transmission & Data Reception, For Multiplication of Two Signal We use X-OR Gate. In X-OR Gate, When Two Similar Signal ie.'0'-'0' or '1'-'1'. Then its Output Signal is always '0'. While Two Dissimilar Signal ie.'0'-'1' or '1'-'0'. Then its Output Signal is always '1'.

In the proposed system we are going to send the data by XORing the data with Walsh sequence generated and at the receiver state we will be comparing the data with the wash and comparing the output which is depicted in the following figure:

Transmitter & Receiver of Walsh System

**Figure 1** Walsh Sequence as carrier signal for CDMA Transmitter and Receiver

As observed from the above figure the data is taken as input, the proposed data input limit is 7 bits. The transmitter takes the data as input and XOR it with the Walsh sequence. The proposed limit of Walsh sequence is 7 bits finally the outputSequence is 35 bits. The Example of Transmitted data is as follows

- Data to transfer: 11001 , Walsh sequence: 1011001
- The transmitted data after XORingisTx = 0100110 1011001 1011001 0100110 0100110
- This data is then taken as the receiver and again the XORing is done with the Walsh sequence.
- Received Data: 0100110 1011001 1011001 0100110 0100110, Walsh sequence: 1011001
- Processed Data: 1111111 0000000 0000000 1111111 1111111
- Now this processed data is sent to a comparator. The comparator is a logic from which the 35-bit output bit is processed and then changed to the 5-bit original data. In this comparator, the bits are compared if the number of 1 is more in the set the data is taken as 1 same if the 0 is in dominance in the set it is converted to 0 for example.
- 1111111 = 1, 1111111 = 1, 1001111 = 1, 0001001 = 0, 0000001 = 0
- Similarly, if we recreate our data we get the input 11001 back.

Walsh Sequence Generator

If the Walsh sequence is fixed the security of the communication can be easily compromised as if the sequence is leaked then the data can be regenerated. Therefore we have to keep the Walsh sequence dynamic which can be generated at runtime. For this we are using two 32 bit registers as observed in the following figures:

Walsh Sequence Generation
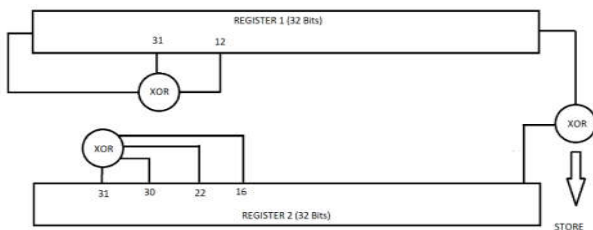
Figure 2 Here 2No's of 32 bit register is Xoring with each other & generate runtime walsh sequences.

As observed from the above figure there are two 32 bits present to generate the Walsh sequence the basic register bits are XORed with each other. The basic of register 1 is 11111111100001111000011111100001.

The basic value if register 2is 11111111111001111111101111111110011. In register 1 the bit number 12 and 31 is XORed with each other and the bit is passed on 31st place making a right shift. Similarly, for the register 2, number 16, 22, 30 and 31 are XORed with each other and the value is passed on to bit 31 and again right sift is performed.

Once the shift is done the new value of both the registers are XORed with each other and is stored in the register.

Walsh Gold Code Generation Algorithm

Step 1: The registers are set to its initial value.
Step 2: The 12th and 31st bit of register 1 are XORed and is passed onto the 31st bit creating a right shift.

Step 3: The 16th, 22nd, 30th, and 31st bit of register 2 are XORed with each other and is passed onto 31st bit creating a right shift again.
Step 4: Now, the values of both the registers are XORed with each other to create the WALSH code and is stored in a register.

Walsh Sequence Generation Implementation

As observed from the proposed methodology the block diagram of the proposed system is as follows:

Block Diagram of Walsh System
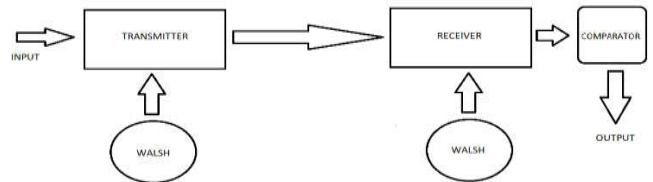
Figure3 Receiver output pass through comparator and generate output signal

As observed the figure illustrates the block of the proposed system, the system takes a 5-bit input 11000. This data is given input to the transmitter. Then at runtime, the system generates the Walsh sequence such as 1010101. Now the Data and Walsh Sequence are XORed and the Data to be Sent is as Follows

Tx = 0101010 0101010 1010101 1010101 1010101
This data is then sent to the receiver. It takes this input and again this sequence is XORed with Walsh sequence.
Rx = 0101010 0101010 1010101 1010101 1010101
*Sx* = 1010101 1010101 1010101 1010101 1010101
D = 1111111 1111111 0000000 0000000 0000000

Now, this data is sent to the comparator for comparison and finally, the data received is 11000. While comparing if instead of all 1's or all 0's we get some other output such as 11110 or 01010 then the occurrence of 0 or 1 is taken into account that is if the number of 1 is more than the selected bit is 1 similarly in the example two the number of 0 is more than the selected bit is 0. The Function of Comparator is only decode data in terms of '1' or '0'. It decode set of sequence with only More no of bit as '1' or '0' and finally decode its to output Signal. If any bit at the input of Comparator is '1' in terms of '0', then it does not change its output, It output Totally depend on More no of '0' or '1'. This comparator helps in error correction as if one or two bits of data is added with noise still we can generate our original data. So We can conclude that Walsh Sequence is Error Detecting and Correcting Mechanism. Also this system has High Throughput(Packets per Second) than other.

RESULT

While, When we Design Full System of Walsh System in CDMA Implementation at that time, it Design in X-links ISE 9.1 I Software . So, Below are the Figures of Waveform of Full system.

Walsh Sequence Waveform of System with CDMA
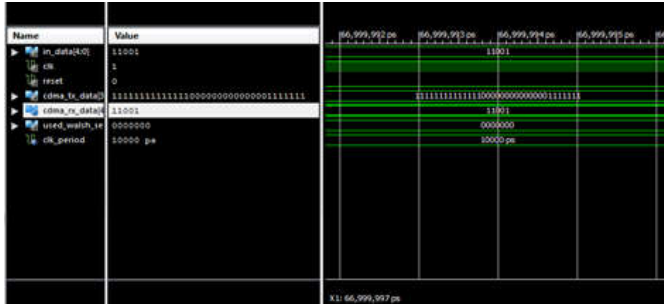
**Figure 4**ThisWaveform shows Equal Receiver and Transmitter signal when it passes to random walsh sequences.

So, When we Design CDMA Tx, Rx and Walsh Seq generator in same system, then We found that Input Seq 11001and Receiver O/P Seq 11001 are same. So, we conclude that data is transmitted from Tx to Rx.
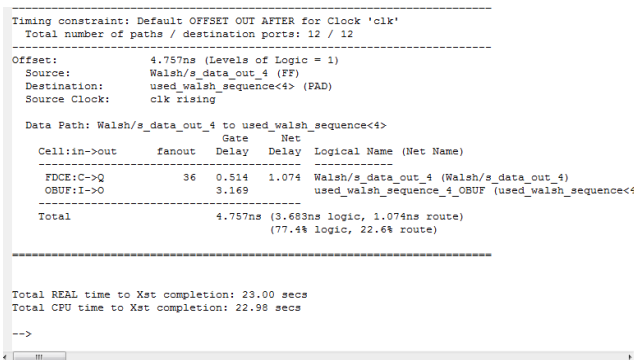
RTL Schematic_1 of Walsh Sequence System with CDMA

Figure 5Here Clock,Reset signal applied with input data and Gives Receiver output when applyingWalsh Sequences.

RTL Schematic_2 of Walsh Sequence System with CDMA
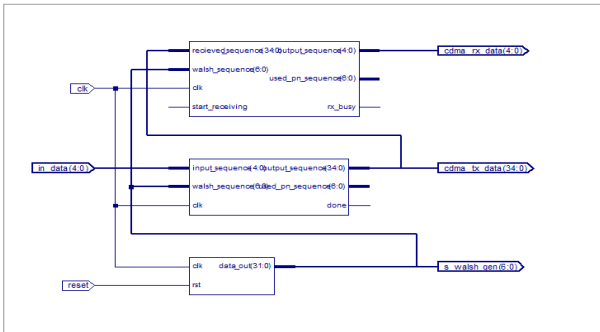
Figure 6: It gives details about all signal which is used in whole system

Delay recorded of the Proposed Walsh Sequence System

Figure 7 Above Figure shows total transaction time & delay for whole system

As observed from the above figure the Walsh is requiring a delay of 1.074ns to generate the 32 bit sequence and 4.757ns as the total transaction time**.**

Power recorded of the proposed Walsh Sequence System

Figure 8 Here it shows Dynamic and Quiescent Power for whole system for 1MHZ input frequency

As observed from the above figure while running the system on 1MHZ the dynamic power required is 0.10W.

DISCUSSION

In this section of the paper, we are going to analyse our proposed model with the implemented base model proposed by GuravPurohit, V. K. Chaubey, KotaSolomanRaju and DivyaVyas [1]. The table below compares the power and delay of the proposed system with the base system.

Table 1 Comparision of Time Delay and Power Between Base System & Proposed System

Parameter	Base System	Proposed System
Delay (in ns)	1.667	1.074
Power (w)	0.470	0.1

As observed from the above table the delay and power is optimized to a great extent as the system reduces nearly 600ns of delay and the power to 0.3 watt which is a considerable amount therefore we can say that our system is better than the base system in terms of security, delay and power.

CONCLUSION

In this paper, the study of enhancing the security of transmission is studied where the security is enhanced using Walsh sequence which is applied to the transmitter and receiver. Traditionally the system uses a static Walsh sequence in which the sequence is static which can compromise the security if the sequence is known to the attacker. To overcome this problem we are generating the Walsh sequence atruntime. To generate the sequence we are using two 32 bit registers which are loaded with some default values. To generate the sequence, two bits of register 1 i.e. 31st and 16th are XORed with each other and then passed to 31st bit again making a right shift. Similarly, the bits of register 2 namely 16, 22, 30 and 31st are XORed with each other and then passed on 31st making a right shift not the value of registers are XORed and used as the random sequence required at runtime. So, this system has High Throughput(Packets per second) than other.The second constraint of the traditional system was the error correction to overcome this issue the introduction of the comparator is done which helps in correcting the errors. In this system, the power and area of the traditional system are also enhanced by the use of runtime sequence generation. The observed value of delay and power recorded are 1.074ns and 0.10W which is lower than

that of the base system studied. Hence the proposed system is better in terms of security, delay and power dissipation than the base system.To improve security using advanced source coders. It also used with low density parity checkers.

References

1. Gurav Purohit, V. K. Chaubey, Kota Soloman Raju and Divya Vyas, " FPGA based Implementation & Power Analysis of Parameterized Walsh Sequence", IEEE, 2014.
2. R.Steele: "Introduction to Digital Cellular Radio," in R.Steele and L.Hanzo (eds), "Mobile Radio Communications, " 2nd ed., IEEE Press, New York, 1999.
3. H.F. Harmuth: "Transmission of Information by Orthogonal Functions," Springer-Verlag, Berlin, 1970.
4. A.Duel-Hallen, J.Holtzman, and Z.Zvonar: "Multiuser Detection for CDMA Systems," IEEE Personal Communications, April 1995, pp. 46-58.
5. Martin Cooper, Marc Goldburg, "Intelligent Antennas: Spatial Division Multiple Access" Annual Review of Communications,1996.
6. 3GPP, Third Generation Projtect Partership, www.3gpp.org (accessed 20/11/01) M. Young, The Technical Writer's Handbook. Mill Valley, CA: University Science, 1989.
7. B. J. Wysocki, T. A. Wysocki, "Modified Walsh-Hadamard Sequences for DS CDMA Wireless System" University of Wollongong
8. D.R.Anderson and P.A.Wintz: "Analysis of a spread-spectrum multiple-access system with a hard limiter," IEEE Trans. on Commun. Techn., vol. COM-17, pp.285-290, 1969.
9. Rayleigh Fading Channels in Mobile Digital Communication Systems Part I: Characterization‖, IEEE Communications Magazine,July 1997.
10. T.S.Rappaport. Wireless Communications –principles and practices, 2nd Edition,(2002 by Prentice-Hall), Upper Saddle River, New Jersey. Ch.5.
11. J.Proakis;- Digital Communications‖, McGraw-Hill, 4th Edition,2001.
12. Simon Haykin,- Communication Systems‖, 4th edition,2001, John Willey & Sons, Inc.
13. L.R.Welch: "Lower bounds on the maximum cross-correlation of signals," IEEE Trans. Inform. Theory, vol. IT-20, pp. 397-399, 1974.

****